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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/342,801	06/29/1999	KLEIN L. JOHNSON	15436.434.5	7109

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EXAMINER	
MOONEY, MICHAEL P	
ART UNIT	**PAPER NUMBER**
2883	

DATE MAILED: 01/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/342,801	JOHNSON, KLEIN L.	
	Examiner	Art Unit	
	Michael P. Mooney	2883	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,7,33-49,55-62,64 and 65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,7,33-49,55-62,64 and 65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Further analysis indicates that claims 1, 33 should not have been indicated as allowable subject matter over Noddings et al. Examiner regrets this oversight. Detailed reasoning appears in the rejection below.

The cancellation of 12, 14-17, 24-27, 66-68 is acknowledged.

Election/Restrictions

In accordance with the statements made in the first paragraph of the *Election/Restrictions* section of the 4/9/04 Office action, excluding claims 12, 14-17, 24-27, 66-68 which were cancelled after the Nemoto et al. rejection in the 4/9/04 Office action, the claims elected by the Applicant are 1-3, 5, 7, 33-49, 55-62, and 64-65.

Claims 1, 12, 24, 33 link(s) inventions Group I and Group II. The restriction requirement between the linked inventions is subject to the nonallowance of the linking claim(s), claims 1, 12, 24, 33. Upon the allowance of the linking claim(s), the restriction requirement as to the linked inventions shall be withdrawn and any claim(s) depending from or otherwise including all the limitations of the allowable linking claim(s) will be entitled to examination in the instant application. Applicant(s) are advised that if any such claim(s) depending from or including all the limitations of the allowable linking claim(s) is/are presented in a continuation or divisional application, the claims of the continuation or divisional application may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Where a restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no

longer applicable. *In re Ziegler*, 44 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Since claims 1, 33 are no longer considered allowable per the below rejection, claims 8-11, 50-54 are no longer rejoined for examination at this juncture.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-3, 5, 7, 33-49, 55-62, and 64-65 are rejected under 35 U.S.C. 103a as being unpatentable over Noddings et al. (5574814).

Regarding claim 33, Noddings et al. teaches a chip-scale package (see fig. 2 below infra.) for photonic devices including a transparent window 114 (fig. 1) having at least one conductive trace patterned on a surface of said window (col. 5 lines 1-7).

Although Noddings et al. does not explicitly state "semiconductor chip", it would have been obvious to do so because it is notoriously well known (NWK) to integrate VCSEL(s) as part of a semiconductor chip.

One of ordinary skill in the art at the time the invention was made would have been motivated to integrate VCSEL(s) as part of a semiconductor chip for the purpose of efficient, reliable production/packaging/integration of the devices.

Noddings et al. teaches a VCSEL/semiconductor chip fixed relative to said window (col. 4 lines 1-3) having at least one terminal connected to the at least one conductive trace (col. 5 lines 1-7); a first housing surrounding said VCSEL/chip and affixed to said window (see fig. 2 below infra.; col. 4 lines 1-3; col. 5 lines 14-18); and a conductive path from the at least one conductive trace to an at least one pad/wire assembly 130 on an external surface of said enclosure. (See the following two paragraphs below infra.).

Regarding claim 33, Noddings et al. col. 5 lines 1-7 states that the flex 116 can be connected to metallized circuit traces within Sapphire window instead of directly to VCSEL 115. Furthermore, Noddings et al. col. 5 lines 1-7 states that the connection from VCSEL 115 to flex 116 by wire bond/flipchip/TAB connections from the VCSEL 115 to the metallized traces on the sapphire window 114.

Furthermore, Noddings et al. col. 4 lines 16-25 states that VCSEL(s) 115 are electrically bonded to electrical circuit components 131 via wire assembly 116. Additionally, Noddings et al. col. 4 lines 26-35 states that the circuit block 131 contains various electrical components and that external electrical access to the electrical circuit

components within circuit block 131 is provided by wire assembly/pad 130 (fig. 2). Thus, a continuous electrical connection or "conductive path" from the at least one conductive trace (col. 5 lines 1-7) to the wire assembly/pad(s) 130 occurs in Noddings et al.'s invention.

Thus claim 33 is rejected.

Regarding claim 1, Noddings et al. teaches a chip-scale package for photonic devices including a window 114 having one or more conductive traces on a first side of said window (col. 5 lines 1-7); a VCSEL/chip fixed relative to the first side of said window (col. 4 lines 1-3; fig. 2); a first housing (see orange in fig. 2 below infra.) extending around said chip and fixed relative to said window (see fig. 2 below infra.; col. 4 lines 1-3; col. 5 lines 14-18); said VCSEL/chip having one or more electrical terminals (col. 4 lines 16-21; col. 5 lines 1-7); said first housing having one or more electrical terminals (fig. 2; col. 4 lines 33-35).

Furthermore, although Noddings et al. does not explicitly state "bump bonded", it would have been obvious to do so because Noddings et al. does teach connection via flipchip (col. 5 lines 4-7) and it is notoriously well known to make flipchip connections via bump bonding.

One of ordinary skill in the art at the time the invention was made would have been motivated to make flipchip connections via bump bonding for the purpose of efficient, reliable production/packaging/integration of the devices.

Noddings et al. teaches at least one terminal of said VCSEL/chip being bump/flipchip bonded to a conductive trace on said window, and at least one terminal

of said first housing 129 (see orange in fig. 2 below infra.) being bonded to a conductive trace on said window 114 (fig. 2; #116; col. 6 lines 51-54 & col. 5 lines 1-7; or col. 5 lines 14-19 & col. 5 lines 1-7).

Although Noddings et al. does not explicitly state that the housing 129 is "bump" bonded, Noddings et al. does teach the housing 129 being bonded to a conductive trace on said window (col. 6 lines 51-54 & col. 5 lines 1-7; or col. 5 lines 14-19 & col. 5 lines 1-7). Therefore, it would have been obvious for Noddings et al. to state "bump" bonding because it is notoriously well known (NWK) to use "bump" bonding with the bonding techniques stated (i.e., at col. 6 lines 51-54 & col. 5 lines 1-7; or col. 5 lines 14-19 & col. 5 lines 1-7).

One of ordinary skill in the art at the time the invention was made would have been motivated to use "bump" bonding with the bonding techniques stated for the purpose of efficient, reliable production/packaging/integration of the devices.

Thus claim 1 is rejected.

Noddings et al. teaches said chip is hermetically sealed by said window and said first housing (figs. 1 & 2; col. 3 lines 54-60; col. 4 lines 1-10; col. 8 lines 45-52). Thus claim 2 is rejected.

Noddings et al. teaches the package of claim 2, wherein said first housing is sealed to said window at the periphery of said window by a sealing-type material. (figs. 1 & 2; col. 3 lines 54-60; col. 4 lines 1-10; col. 8 lines 45-52). Thus claim 3 is rejected.

Noddings et al. teaches the package of claim 1, wherein said chip/VCSEL comprises a photonic device. (see fig. 2 below infra.; col. 4 lines 1-3; col. 5 lines 14-18). Thus claim 5 is rejected.

Noddings et al. teaches the package of claim 5, further comprising a second housing 108 situated adjacent to a second side of said window. (figs. 1 & 2). Thus claim 7 is rejected.

By the above reasons and references each and every element of claims 34, 55 are taught by Noddings et al. Thus claims 34, 55 are rejected.

Although Noddings et al. does not expressly teach the window has at least one feature on the surface of window for alignment, it would have been obvious to expressly state this because it is NWK for a window to have at least one feature on the surface of said window for alignment.

One of ordinary skill would have been motivated to include at least one feature on the surface of window for alignment in order to increase coupling efficiency. Thus claim 35 is rejected.

By the above reasons and references each and every element of claims 36-38 are taught by Noddings et al. Thus claim 36-38 are rejected.

By the above reasons and references each and every element of claim 39, 42-43, 48-49 are taught by Noddings et al. Thus claims 39, 42-43, 48-49 are rejected.

Noddings et al. teaches such a use of a solder type material at col.5 lines 14-18. Thus claim 40 is rejected.

Furthermore, each and every element of claim 41 is rejected because it is NWK to use an adhesive-type material in such an application. Thus claim 41 is rejected.

Each and every element of claims 44-47 are rejected because it is NWK to use a refractive/diffractive optical element in such application(s).

One of ordinary skill would have been motivated to use a refractive/diffractive optical element as stated in the claim(s) in order to increase coupling efficiency. Thus claims 44-47 are rejected.

By the above reasons and references each and every element of claim 55 is taught by Noddings et al. Thus claim 55 is rejected.

By the above reasons and references and the fact that Noddings et al. teaches a ceramic at col.4 lines 50-55 each and every element of claim 56 is rendered obvious by Noddings et al. Thus claim 56 are rejected.

Noddings et al. teaches a sapphire window at, e.g., col. 4 line 1. Although Noddings does not expressly teach a quartz window, this would have been obvious because it is notoriously well known (NWK) that quartz and sapphire are alternately usable in such applications. Thus claim 57 is rejected.

One of ordinary skill would have been motivated to interchange quartz for sapphire in order to increase coupling efficiency in a given application. Thus claim 57 is rejected.

By the above reasons and references each and every element of claims 58-59 are taught by Noddings et al. Thus claim 58-59 are rejected.

Noddings et al. teaches the package of claim 59, wherein said first housing is a multi-layer housing (fig. 2), and the at least one terminal of said first housing is electrically connected to a terminal 130 outside of said first housing via a trace (see inside end of 130) in the multi-layer housing. (fig. 2; see orange in fig. 2 below infra.). Thus claim 60 is rejected.

Claim 61 is rejected because there is more than 1 trace in the group/array of terminals 130. (fig. 1). Thus claim 61 is rejected.

Noddings et al. teaches a chip-scale package for photonic devices (fig. 2 below infra.), comprising: a window 114; a chip fixed relative to a first side of said window (figs. 1-2; #115); a first housing (see orange in fig. 2 below infra.) having a body with an outer surface and an inner surface, the inner surface extending around said chip and fixed relative to said window to form a chip cavity (fig. 2); said first housing having at least one electrical terminal 130 along its outer surface, which is electrically connected through the body of the first housing to at least one electrical terminal (where 116 joins housing component 129) along the inner surface of the first housing; said window 114 includes one or more conductive traces (col. 5 lines 1-7); said chip 115 includes one or more electrical terminals (col. 5 lines 1-7); and at least one terminal of said chip is bonded to a conductive trace on said window (col. 5 lines 1-7), and at least one terminal 116 along the inner surface of the first housing is bonded to a conductive trace on said window.

Furthermore, although Noddings et al. does not explicitly state "bump bonded", it would have been obvious to do so because Noddings et al. does teach connection via

flipchip (col. 5 lines 4-7) and it is notoriously well known to make flipchip connections via bump bonding.

One of ordinary skill in the art at the time the invention was made would have been motivated to make flipchip connections via bump bonding for the purpose of efficient, reliable production/packaging/integration of the devices.

Thus claim 62 is rejected.

Noddings et al. teaches the package of claim 62, wherein the at least one terminal of said chip is bump bonded to the same conductive trace as the at least one terminal of said first housing. (col. 5 lines 1-7). Thus claim 64 is rejected.

Noddings et al. teaches the package of claim 62, wherein said first housing is a multi-layer housing. (see orange in fig. 2 below infra). Thus claim 65 is rejected.

Key: ▭ - 1st housing extending around chip (orange)
▭ - hermetically sealed region (green)

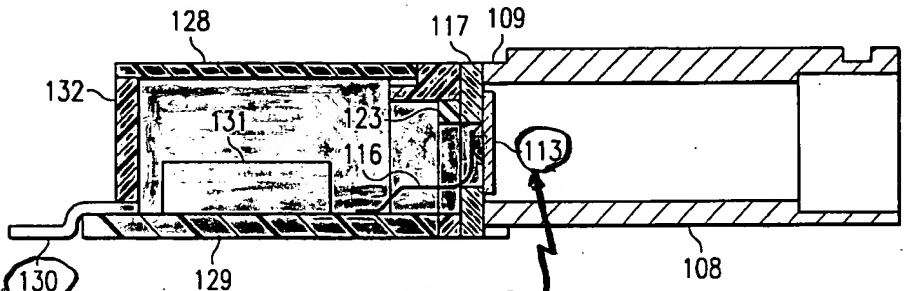

FIG. 2

wire assembly #130

VCSEL #115 ▭ (purple) bonded to Sapphire Wafer Window #114 ▭ (yellow) (See col. 3 lines 60-65)

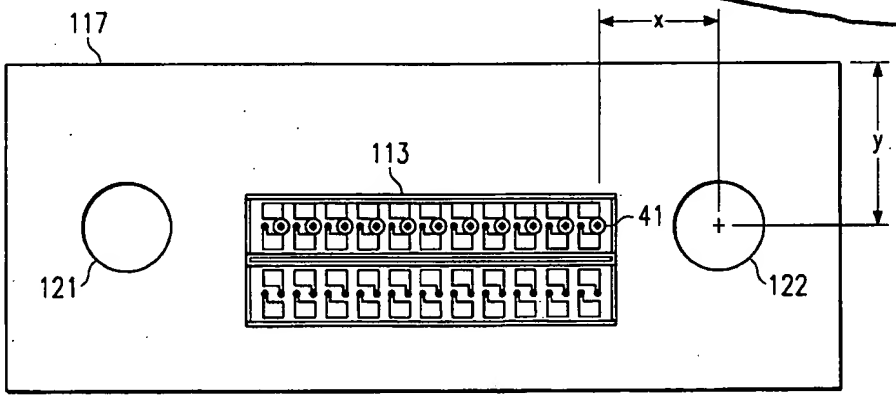

FIG. 4

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Corzine et al. (6188711), Haerle (6100104), Huang et al. (6097748), Geng (6064423), Jewell (5940964), Ramdani et al. (5898722), and Chirovsky (6222206) teach integrating VCSEL(s) as part of a semiconductor chip. Additionally, Jewell (5940564), Ichino et al. (6071016), and De Dobbelaere et al. (6097871) among numerous other references show making flipchip connections via bump bonding. Finally, Brady et al. (6100804), Sawamura et al. (6303219), Farnworth (6097087), Seppala et al. (5665639), Urushima (5662263), Wang et al. (5587336), Asanasavest (5230458) are additional references which illustrate the interchangeability of various bonding techniques to be used with bump bonding.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael P. Mooney whose telephone number is 571-272-2422. The examiner can normally be reached during weekdays, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank G. Font can be reached on 571-272-2415. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

Michael P. Mooney
Examiner
Art Unit 2883

Frank G. Font
Supervisory Patent Examiner
Art Unit 2883

FGF/mpm
12/28/04